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1 1. (Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said
2 method comprising:

3 determining when a first-type of signal is present on an input to a logical gating device,
4 wherein said first-type of input signal allows transitions on an output of said gating device;

5 determining when a second-type of signal is present on said input, wherein said
6 second-type of input signal inhibits transitions on said output of said gating device; and

7 modifying a timing of a sensing of said first-type of signal to sense said first-type of
8 signal at an earlier point in time than said second-type of signal is sensed.

1 3. (Amended) The method of claim 1, wherein:

2 said input comprises a clock input;

3 said first-type of signal and said second-type of signal comprise clock trailing edge
4 signals;

5 said first-type of signal causes a transition at said output of said gate device due to a
6 transition on a gate input of said gate device; and

7 said second-type of signal prevents a transition at said output of said gate device.

1 4. (Amended) The method of claim 2, wherein said first-type of signal [prevents] allows
2 said clock pulses to be propagated on said output of said gating device and said second-type of
3 signal prevents said clock pulses from being propagated on said output of said gating device.

1 11. (Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said
2 method comprising:

3 determining when a first-type of signal is present on an input to a logical gating device,
4 wherein said first-type of input signal allows a clock pulse to be output from said gating device;

5 determining when a second-type of signal is present on said input, wherein said
6 second-type of input signal inhibits said clock pulse from being output from said gating device;
7 and

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8 modifying a timing of a sensing of said first-type of signal to sense said first-type of
9 signal at an earlier point in time than said second-type of signal is sensed.

1 17. (Amended) A program storage device readable by machine, tangibly embodying a
2 program of instructions executable by said machine for performing a method of evaluating gate
3 timing in an integrated circuit (IC) design, said method comprising:

4 determining when a first-type of signal is present on an input to a logical gating device,
5 wherein said first-type of input signal allows transitions on an output of said gating device;

6 determining when a second-type of signal is present on said input, wherein said
7 second-type of input signal inhibits transitions on said output of said gating device; and

8 modifying a timing of a sensing of said first-type of signal to sense said first-type of
9 signal at an earlier point in time than said second-type of signal is sensed.

1 19. (Amended) The program storage device of claim 18, wherein said first-type of signal
2 allows said clock pulses to be propagated on said output of said gating device and said
3 second-type of signal prevents said clock pulses from being propagated on said output of said
4 gating device.